Amendments to the Specification:

Please replace the paragraph beginning on page 7, line 14 with the following amended paragraph:

In the DDR 226 specification, the CLK period is 7.5 ns, t_{WR} and t_{RP} are both 2 CLK periods (15 ns) in duration, and t_{TOT} is 4 ~~clock~~ CLK periods (30 ns) in duration. In the DDR 333 specification the CLK period is 6.0 ns, t_{WR} is 2 CLK periods (12 ns) in duration, t_{RP} is 3 CLK periods (18 ns) in duration, and t_{TOT} is 5 CLK periods (30 ns) in duration. Note however, that the internal timings, t_{WRT} and t_{EQL}, are the same for both cases. This is accomplished by timer lockout circuit 140. (see FIG. [[2]] 3) delaying the end of t_{WRT} relative to [[,]]≤PC> by 3 ns